Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the applications.

Listing of Claims:

1. (Currently Amended) A high performance network address processor comprising:

a longest prefix match lookup engine for receiving a network address request having a designated network destination address; and

an associated data engine coupled to the longest prefix match lookup engine ~~for~~ that is capable of receiving a key and an output address pointer from the longest prefix match lookup engine and that is capable of providing a network address processor data output corresponding to the designated network ~~destination~~ address pointer.

2. (Original) The high performance network address processor of claim 1 wherein the longest prefix match lookup engine comprises a plurality of pipelined lookup tables.

3. (Original) The high performance network address processor of claim 1 wherein the network address processor is configurable to a variety of destination address width.

4. (Original) The high performance network address processor of claim 1 wherein the network address processor generates a network address data output in one clock cycle.

5. (Currently Amended) A high performance network address processor integrated circuit, wherein the network address processor integrated circuit comprises:

a longest prefix match lookup engine for receiving a network address request having a designated network destination address; and

an associated data engine coupled to the longest prefix match lookup engine ~~for~~ that is capable of receiving a key and an output address pointer from the longest prefix match lookup engine and that is capable of providing a network address processor data output corresponding to the designated network ~~destination~~ address pointer.

6. (Original) The high performance network address processor of claim 5 wherein the longest prefix match lookup engine comprises a plurality of pipelined lookup tables.

7. (Original) The high performance network address processor of claim 2 wherein the plurality of pipelined lookup tables is implemented in a DRAM.

8. (Original) A high performance network addressing method comprising the steps of:

providing a longest prefix match lookup engine with a network address data request and a destination network address, wherein the longest prefix match lookup engine comprises a set of lookup tables;

searching the set of lookup tables to select a look up engine address output from the set of lookup tables to provide to an associated data engine; and

searching the associated data engine to provide an associated destination address data output.

9. (Original) The high performance network addressing method of claim 8 wherein the step of searching the set of lookup tables comprises searching for an entry of the set of lookup tables that comprises the smallest entry that is greater than or equal to an input search key, the step of searching for the smallest entry comprising the steps of: selecting the smallest entry that equals the input search key with a corresponding number of mask bits,

wherein if one or more entries comprise the same key, the key having the smallest mask is selected, and

wherein if no key matches the above requirements, the maximum key in a row is compared with the input search key using each of a set of mask pointer pairs, each of the pointer is selected to correspond to the smallest mask for which the input search key equals the maximum key in the row with the corresponding number of mask bits ignored.